Amendments to the Specification:

Please replace paragraph [0033] with the following amended paragraph:

[0033] Fig. 6 is a simplified high-level block diagram of a PPE 500, in accordance with one embodiment of the present invention, coupled to a general purpose CPU 508, and a memory 10, such as a DRAM and/or flash memory 510. PPE 500 is shown as including a load sharing demultiplexer 502, sixteen vector engines 504, and a multiplexer 506. It is understood, however, that in other embodiments, PPE 500 may include more or fewer than sixteen vector engines 504. As shown in Fig. [[7]] 6, each vector engine 504 is further adapted to include a Discrete Fourier Transform (DFT) engine and a matrix multiplication engine.

Please replace paragraph 0037 with the following amended paragraph:

[0037] As described above, Fig. 7 is a simplified high-level simplified block diagram of an image processing 400, in accordance with one embodiment of the present invention. Image processing 400 is shown as including, in part, a camera unit 405, a high-speed high-performance interconnect module 410, such as a PCI-X or 3GIO card, and host mainboard 420. Interconnect module 410 is further configured to include, in part, a realignment unit and frame buffer 412, one [[ore]] or more IPE 200, and one [[ore]] or more PPE 500. Host mainboard 420 is further configured to include, in part, a host DRAM 416, a high performance interconnect module 424, such as a PCI-X or 3GIO NorthBridge 424, and a host CPU 426. It is understood that each camera unit 405 may include a CCD (or other image capturing devices) as well as one [[ore]] or more ADCs.